CALIFORNIA STATE POLYTECHNIC UNIVERSITY, POMONA

ETE 230

COURSE OUTLINE

Course Information		**ABET Unit Classification** (4 Quarter Units)	
Department:	Engineering Technology	Math:	
Course Number:	ETE 230/230L	Basic Science:	
Course Title:	Introduction to Digital Logic/Lab	Engineering Topics:	4
Revision Date:	3/20/05	*Contains significant design content:*	Yes
Revised by:	Massoud Moussavi	Other:	
Compliant:	Catalog 2004/05	Curriculum Designation:	Required

I. Catalog Description

Introduction to Digital Logic ETE 230/ETE 230L (3/1)
Study of numbering systems and their conversions; Theory and practice of fundamental and universal gates and their SOP and POS interconnections and their conversion; Simplification theories; Theory, design, and applications of MSI and LSI logic devices including adders, comparator, multiplexers; Introduction to the programmable logic devices (PLDs).;Practice, design, and simulate digital logic network using B2SPICE, PSPICE and Altera software. 3 lectures/problem solving and 1 three-hour laboratory. Prerequisite: ETE 103.

II. Prerequisites and Corequisites

ETE 103 and MAT 105 are co-requisites.

III. Textbook and/or other Required Material

Morris Mano, Digital Design, Third Edition, Prentice Hall Publication Co.

IV. Course Objectives

Upon successful completion of this course, each student should be able to:

1. Describe numbering systems and their conversions.
2. Explain the combinational SOP and POS logic circuits and their applications.
3. Use any simplification method such as K-Map to minimize the output Boolean expression.
4. Implement logic circuits to perform arithmetic and logic operations of binary, hexadecimal, and BCD, code and code conversion.
5. Explain and analyze the functions and applications of logic devices such as Adders, Comparators, Encoders, Decoders, Multiplexers, and Demultiplexers.
6. Explain and analyze the functions and applications of PLDs.
7. Design, test, and simulation of variety combinational logic networks using B2Logic, PSPICE, and Altera's MAX + Plus II software.

V. Expanded Course Description

A. Expanded Description of the Course

1. Numbering systems

Introduction to numbering systems such as: Binary, Octal, Hexadecimal, and BCD and their conversions. (1 week)

2. **Logic gates**
Characteristics and applications of logic gates: Inverter, AND, OR, NAND, NOR, XOR, and XNOR. (1 week)

3. **Combinational logic networks**
Characteristics and applications of combinational logic circuits: SOP and POS and their conversion. (1 week)

4. **Boolean algebra and simplification methods**
Simplification methods of Boolean expression such Boolean algebra and K-map for 3-to-5 input logic networks. (2 weeks)

5. **Arithmetic and Logic operations**
Study of arithmetic and logic operation of: Binary, Hexadecimal, and BCD numbers and their logic devices and networks, code and code conversions. (2 weeks)

6. **Logic devices**
Characteristics of logic devices such as: Adders, Comparators, Parity generator & checker, Encoders, Decoders, Multiplexers, and De-Multiplexers and their applications. (2 weeks)

7. **Programmable Logic Devices (PLDs)**
Introduction to Programmable Logic Devices Such as: ROM, PAL, PLA, and GAL. (1 week)

B. Typical Laboratory Experiments

Lab 1. Design, analyze, test, and simulation of a Sum-Of-Product logic network.

Lab 2. Design, analyze, test, and simulation of a Product-Of-Sum logic network.

. Lab 3. Design, analyze, test, and simulation of a 4-input logic network using K-map.

Lab 4. Design, analyze, test, and simulation of an arithmetic logic network using Adder/Subtractor

Lab 5. Design, analyze, test, and simulation a parity generator and Parity checker.

Lab 6. Design, analyze, test, and simulation of a logic network to perform code conversion from "8421" code to a Gray-code and/or Ex-3 code and visa-versa.

Lab 7. Design, analyze, test, and simulation of a logic network using Encoder and/or Decoder.

Lab 8-9. Final laboratory project; Design, analyze, test, and simulation of a combinational logic circuit using MUX, and/or De-MUX, or PLD.

VI. Class/Laboratory Schedule

Lecture: Two 75 minute sessions per week.
Lab: One 3 hour session per week.

VII. Contribution of Course to Professional Component

Lecture: Students learn about analyze and design combinational logic devices and networks including Small-Scale and Medium-Scale Integrated Circuits and their applications.

Lab: Students learn how to design, build, simulate, test, and troubleshoot the variety of combinational logic networks in both hardware and software laboratories. They also learn how to write a technical report based on collected data. A wide range of measurement techniques is used in lab exercises including B2Spice, PSPICE, and Altera's MAX +Plus II software tools.

VIII. Evaluation of Students

The instructor evaluates outcomes using the following methods: homework assignment submittals, midterm and final exams, one-on-one discussions during office hours, laboratory experiments, and laboratory reports.

The student grades are typically based on the following factors: quizzes, homework, midterm exam and final Exam.

IX. Relationship of Course Objectives to Program Outcomes

Crse Obj	Program Outcomes										
	(a) **Use of modern tools of discipl**	***(b)*** **Use of math, science, Engg & Tech**	***(c)*** **Do experi-ments**	***(d)*** **Dsn of sys & components**	***(e)*** **Work on teams**	***(f)*** **Do Tech probs**	***(g)*** **Eff Com**	***(h)*** **Life-long learn**	***(i)*** **Prof, ethics, social resps**	***(j)*** **Prof, soc, globl, diversity**	***(k)*** **Qual, Cont impr, timeliness**
1		X				X					
2				X		X					
3				X		X					
4		X		X		X					
5		X		X		X					
6	X			X		X					
7	X		X	X	X	X	X	X			