CALIFORNIA STATE POLYTECHNIC UNIVERSITY, POMONA

ETE 315/315L

COURSE OUTLINE

Course Information		**ABET Unit Classification** (4 Quarter Units)	
Department:	Engineering Technology	Math:	
Course Number:	ETE 315/315L	Basic Science:	
Course Title:	Digital Logic Ssystems	Engineering Topics:	4
Revision Date:	3/18/05	*Contains significant design content:*	Yes
Revised by:	Massoud Moussavi	Other:	
Compliant:	Catalog 2004/05	Curriculum Designation:	Required

I. Catalog Description

Study of sequential logic circuit including; latches and flip-flops and applications, state diagram, state table, state machines (Mealy and Moore) design, state reduction, applied design of synchronous and asynchronous sequential logic circuits, state machine design with ASM. 3 lectures/problem-solving and 1 three-hour laboratory Prerequisite: ETE 230

II. Prerequisites and Co-requisites

ETE 230/230L; Students are expected to have a good theoretical, analytical, and practical knowledge of combinational logic networks including fundamental and universal gates, SOP, POS, simplification methods, adder/subtractor, comparator, encode, decoder, MUX, DeMUX, and PLDs.

III. Textbook and/or other Required Material

Morris Mano, Digital Design, Third Edition, Prentice Hall Publication Co. ISBN

IV. Course Objectives

Upon successful completion of this course, each student should be able to:

1. Understanding of clock signal, timing diagram, latches and flip-flops.
2. Understanding of counters and shift registers.
3. Understanding of state table, state diagram, state machines and design processes.
4. Explain the differences between Mealy and Moore machine, their conversion and state reduction methods.
5. Analysis and design of synchronous and asynchronous sequential networks.
6. Analysis and design of complex sequential networks.
7. Understanding of ASM chart and design of sequential network from ASM chart.

V. Expanded Course Description

A. Expanded Description of the Course

1. Clock signaling, timing diagram, latches, and flip-flops
Characteristics of clock signal, timing diagram, latches, RS, D, JK, and T flip-flops with enable, preset, clear, and clock. Study and design of simple sequential network with different flip-flops (2 weeks)

2. Counters and shift registers.

Study and design of variety of counters such as ripple, Johnson, BCD, Mod-2, Mod-6 and their applications. Study and design of all types of shift registers such SISO, SIPO, PISO, PIPO and their applications. (2 weeks)

3. **State table, state diagram, and state machines**
   Characteristics of state table, state diagrams in design a sequential network. Study of Mealy and Moore state machines, their conversion, and state reduction in Mealy and Moore machines (2 weeks)

4. **Complex sequential networks**
   Study and design of complex sequential networks and sequence reading networks, and serial data code conversion. Characteristics of the race, static and dynamic hazards in the sequential logic network. (2 weeks)

5. **Algorithm of State Machine (ASM) chart**
   Characteristics of SAM chart and its individual elements, ASM representation of a sequential logic networks, design of a sequential logic network through ASM chart and using MUX, decoder, ROMs, and CPLDs. (2 weeks)

B. Typical Laboratory Experiments

Lab 1. Design, analyze, test, and simulation of counters.

Lab 2. Design, analyze, test, and simulation of shift registers.

. Lab 3. Design, analyze, test, and simulation of a Mealy machine using D-flip-flops.

Lab 4. Design, analyze, test, and simulation of a Moore machine using J-K flip-flops.

Lab 5. Design, analyze, test, and simulation a Moore machine from a Mealy machine using T-flip-flops.

Lab 6. Design, analyze, test, and simulation a reduced state Mealy machine.

Lab 7. Design, analyze, test, and simulation a sequence reading system.

Lab 8-9. Final laboratory project; Design, analyze, test, and simulation a sequential logic circuit through ASM chart and using MUX, Decoder, and/or PLD.

VI. Class/Laboratory Schedule

Lecture: Two 75 minute sessions per week.
Lab: One 3 hour session per week.

VII. Contribution of Course to Professional Component

Lecture: Students learn about analyze and design sequential logic networks using all types of flip-flops both synchronous and asynchronous types.
Lab: Students learn how to design, build, simulate, test, and troubleshoot the variety of sequential logic networks in both hardware and software laboratories. They also learn how to write a technical report based on collected data. A wide range of measurement techniques is used in lab exercises including B2Spice, PSPICE, and Altera's MAX +Plus II software tools.

VIII. Evaluation of Students

The instructor evaluates outcomes using the following methods: homework assignment submittals, midterm and final exams, one-on-one discussions during office hours, laboratory experiments, and laboratory reports.

The student grades are typically based on the following factors: quizzes, homework, midterm exam and final Exam.

IX. Relationship of Course Objectives to Program Outcomes

Crse Obj	Program Outcomes										
	(a) **Use of modern tools of discipl**	***(b)*** **Use of math, science, Engg & Tech**	***(c)*** **Do experi-ments**	***(d)*** **Dsn of sys & components**	***(e)*** **Work on teams**	***(f)*** **Do Tech probs**	***(g)*** **Eff Com**	***(h)*** **Life-long learn**	***(i)*** **Prof, ethics, social resps**	***(j)*** **Prof, soc, globl, diversity**	***(k)*** **Qual, Cont impr, timeliness**
1		X	X	X		X					
2		X	X	X		X					
3		X	X	X		X					
4	X	X	X	X		X					
5	X	X	X	X	X	X	X	X			