CALIFORNIA STATE POLYTECHNIC UNIVERSITY, POMONA

# ETE 445

COURSE OUTLINE

| Course Information | | ABET Unit Classification (4 Quarter Units) | |
|---|---|---|---|
| Department: | Engineering Technology | Math: | |
| Course Number: | ETE 445/L | Basic Science: | |
| Course Title: | PC-Based Micropro. Sys./Lab | Engineering Topics: | 4 |
| Revision Date: | 10/27/04 | *Contains significant design content:* | Yes |
| Revised by: | Tariq Qayyum | Other: | |
| Compliant: | Catalog 2004/05 | Curriculum Designation: | Required |

## I. Catalog Description

ETE 445/L PC-Based Microprocessor Systems/Lab (3/1)

Microcomputer interfacing; consideration of analog effects upon digital signals. Digital hardware; peripheral equipment and bus standards 3 lecture-problems. 1 three-hour laboratory.

## II. Prerequisites and Corequisites

ETE 344/L. ETE 445 and ETE 445L are corequisite.

## III. Textbook and/or other Required Material

Mazidi/Mazidi, An Introduction to IBM PC's and Compatible Computers

## IV. Course Objectives

The student will be able to:

1. Utilize the 80x86 family of chips to design and implement a working 80x86 computer system via a standard bus.
2. To match components and hardware. Considering timing, loading, and ringing effects.
3. Develop memory and I/O subsystems to communicate with the 80x86 CPU.
4. Understand the consequences of improper grounding and power distribution, and will be able to make effective corrections.
5. Understand the effects of frequency on the propagation of digital signals and to take effective action to correct high frequency anomalies.
6. Analyze bus contention, arbitration and timing problems in parallel bus systems.
7. Interface a UART to a microprocessor based system, and write the programs to transmit and receive date.

## V. Expanded Course Description

A. Expanded Description of the Course

1. VLS1 components and related hardware

   a. The 8088 CPU: min and max modes; pin assignments. The 8282 clock generator: the 8388 bus controller.
   b. System timing: CPU bus cycles, interrupt acknowledgement; the PC standard bus.
   c. Memory and memory system design: address and data buses; buffering; latching; decoding; wait states. DMA, memory-mapped I/O. RAM/ROM interfacing.

2. I/O system design
   a. 8088 port addressing space. Decoders; buffering; latching. Simple I/O applications.
   b. Parallel I/O; the 8255 PPI.
   c. Serial I/O: the 8251 UART.

3. Other related components
   a. The 8254-interval timer.
   b. 8087 math processor.

4. The system monitor.

5. Design of working 80x86 based system.

B. Laboratory Project

The overall objective of this lab is to design and build a working 80x86 computer system on a wire wrap or PC board using the standard family of 80x86 VLSI chips, or equivalent. This includes:

1. Specifying the system type (minimum mode) and related hardware, bus; clock, bus controller, memory (RAM/ROM); I/O serial/parallel/keyboard input, etc.

2. Build the system: perform functional tests.

3. Write the system monitor software.

4. Perform simple I/O: parallel, serial; A-D conversion, etc

## VI. Class/Laboratory Schedule

Lecture: Two 75 minutes sessions per week
Lab: One 3-hour session per week.

## VII. Contribution of Course to Professional Component

Students learn to analyze, design, and develop an understanding of microprocessor-based systems. Students learn to design a working model of 80x86-based system, which includes memory address decoding, memory interfacing, and I/O interfacing. Students also learn to write project report.

## VIII. Evaluation of Students

The instructor evaluates outcomes using the following methods:

- Homework assignment submittals
- Quizzes
- Examinations
- Laboratory project
- Project report

The student grades are typically based on the following factors:
quizzes, homework, midterm exam and final Exam.

## IX. Relationship of Course to Program Outcomes

| Crse Obj | Program Outcomes | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | ***(a)*** **Use of modern tools of discipl** | ***(b)*** **Use of math, science, Engg & Tech** | ***(c)*** **Do experi -ments** | ***(d)*** **Dsn of sys & compo nents** | ***(e)*** **Work on teams** | ***(f)*** **Do Tech probs** | ***(g)*** **Eff Com** | ***(h)*** **Life-long learn** | ***(i)*** **Prof, ethics, social resps** | ***(j)*** **Prof, soc, globl, diversity** | ***(k)*** **Qual, Cont impr, timeli ness** |
| 1 | | X | X | X | | X | | | | | |
| 2 | | X | X | X | | X | | | | | |
| 3 | X | X | X | X | | X | | | | | |
| 4 | | X | X | X | | X | | | | | |
| 5 | X | X | X | X | X | X | X | | | | |